REMARKS

Upon entry of the instant amendment, claims 1-12 are pending. Claims 1 and 9 have been amended to more particularly point out the applicant's invention. In particular, commas have been deleted from element 1c and 9d. With respect to the drawings, the applicant respectfully disagrees with the assertion on page 2 of the detailed action regarding the status of FIG. 7A, 8, 13-15, and 35 and 36. It is respectfully submitted that these figures are all part of the present invention. The examiner's attention is respectfully directed to paragraph [0073].

> "The modeling approach in accordance with the invention is discussed below in connection with FIGS. 5-10. An important aspect of the invention is a measured-to-model microscope (i.e. S-parameter microscope), such as discussed below in connection with FIGS. 11-30 ... One embodiment of such a filter for a Pi-FET-Type layout discussed in connection with FIGS. 26-44."

Thus, it should be clear that FIG. 7A, 8, 13-15, 35 and 36 are part of the present invention and are not part of the prior art. Accordingly, the applicant respectfully requests that the examiner reconsider and withdraw this request.

INFORMATION DISCLOSURE STATEMENT

Paragraph 4 of the Detailed Action states that Japanese document JP 11-330449 was not considered because of a lack of an English translation. It is respectfully submitted that the Japanese patent JP 11-330449A was cited by the U.S. examiner in the corresponding PCT application PCT/US01/13346. Notwithstanding, a machine translation of Japanese publication JP 11-330449 is enclosed. Also enclosed is a patent abstract for Japanese patent publication 11-330449. Both the English abstract and the machine translation were obtained from the website for the Japanese patent office. It is respectfully submitted that Japanese publication JP 11-330449 be made of record.

CLAIM REJECTIONS – DOUBLE PATENTING

Claim 1 has been provisionally rejected under the judicially-created doctrine of double patenting over claim 1 of application no. 09/840,545. In support of the rejection, paragraph 5 of the Detailed Action states: One of ordinary skill in the art can deduce application 09/840,500 is a broad representation of 09/840,545 such that "fabricating," "measuring," "varying predetermined semiconductor devices" are processes identical to "modeling semiconductor devices." It is respectfully submitted that the double patenting rejection must solely be based on the claims of the application itself and not the specification of the application being cited. Accordingly, the examiner is respectfully requested to reconsider and withdraw this rejection.

CLAIM REJECTIONS – 35 U.S.C. § 102

Claims 1-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Biswas ("Modeling and Simulation of High-Speed Interconnects" Dissertation 1998). In order for there to be anticipation, each and every one of the elements must be found in a single reference. It is respectfully submitted that the claims recite elements clearly not taught or suggested by the dissertation. For example, the claims teach establishing a physically-representative equivalent model of one or more characteristics of a semiconductor device; varying the physical characteristics; and correcting the model based upon the measured characteristics.

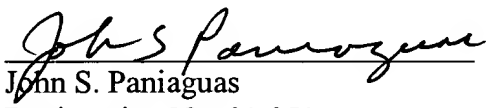
The dissertation thesis simply compares measured experimental results with simulated results using known "canned" software, such as "Fast Cap." The examiner's attention is respectfully directed to the abstract of the dissertation "Results from measurements were compared with the simulation results. The software Layout 2 Fast Cap is available by sending an email to m.b.steer@ieee.org." Thus, it is clear that the dissertation simply compares experimental results with simulated results using canned software. Accordingly, it is respectfully submitted that the Biswas dissertation actually teaches a way from the claims at issue. Thus, the Examiner is respectfully requested to reconsider and withdraw this rejection.

CLAIM REJECTIONS – 35 U.S.C. 103(a)

Claims 5 and 6 were rejected under Biswas in further review of VTT Electronics ("Research Activities and Microelectronics" (2000)). The Biswas dissertation was discussed above. It is respectfully submitted that the VTT Electronics reference likewise does not teach creating a simulation model building a semiconductor device and using test measurements from the semiconductor device to modify the simulation model. For these reasons and the reasons submitted above, the examiner is respectfully requested to reconsider and withdraw the rejection of claims 5 and 6.

Respectfully submitted,

KATTEN MUCHIN ZAVIS ROSENMAN

By: 

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